In the Claims:

The pending claims are presented below.

1. (original) A method of discriminating between different types of scan failures, comprising:

simulating a scan enable signal to a circuit represented by a netlist corresponding to a scan chain coupled to combinatorial logic being tested;

simulating initiating of a data capture cycle in the net list corresponding to the scan chain, the data capture cycle simulating circuit operation to provide simulated output data including a series of scan flops from the scan chain being simulated together with the combinatorial logic; and

scanning data out from each flop in the scan chain and into a test program, the test program: extracting simulated scan flops from the simulated circuit operation data; sorting the simulated scan flops into a logical order; identifying labels for the simulated scan flops; and graphically displaying the simulated scan flops versus time together with the labels.

2. (original) The method of claim 1, the test program further graphically displaying the simulated scan enable signal.

3. (original) The method of claim 1, the test program further forming expected scan output data from the netlist using an automatic test pattern generator and forming a pseudo-signal graphically displaying miscompares between the displayed simulated scan flops and the expected scan output data.

4. (original) The method of claim 1, the test program further forming a pseudo-signal graphically displaying miscompares between the simulated displayed scan flops and expected scan output data.

5. (original) The method of claim 1, wherein extracting the simulated scan flops includes reducing a scope of the simulated output data to one scan chain to be analyzed.

6. (original) The method of claim 1, wherein extracting the simulated scan flops includes reducing the scope of the output data to one scan chain to be analyzed and wherein sorting the simulated scan flops into a logical order includes sorting the simulated scan flops into a logical order extending from scan input to scan output.

8. (original) The method of claim 1, the test program further comparing a selected one of the scan flops to expected scan output data to determine if the selected one of the scan flops agrees with the expected scan output data, and, when the selected one of the scan flops disagrees with the expected scan output data, providing an error message.

9. (original) The method of claim 8, the test program further, after providing an error message, comparing the scan flops to determine if any adjacent two scan flops are identical, and, when two adjacent scan flops are determined to be identical, providing an indication of a transfer problem associated with the two identical adjacent scan flops, and , when no two adjacent scan flops are identical, providing an indication that a capture problem exists.

10. (original) The method of claim 9, the test program further, after providing an indication that a capture problem exists, providing an indication of which scan flop has the capture problem.

11. (original) An article of manufacture comprising:

a computer usable medium having computer readable code embodied therein to cause a display to graphically depict one or more simulated scan output data sets versus time, the computer readable program code in the article of manufacture comprising:

a module to extract the simulated scan flops of one or more scan chains from the simulated scan output data;

a module to sort the extracted simulated scan flops into a logical order;

a module to identify labels for the simulated extracted scan flops; and

a module to graphically display the simulated scan flops versus time together with the labels.

12. (original) The article of manufacture of claim 11, wherein the module to graphically display the simulated scan flops versus time is further configured to graphically display the simulated scan enable signal.

13. (original) The article of manufacture of claim 11, the test program further including a module to form a pseudo-signal including data identifying miscompares between the simulated displayed scan flops and expected signal values, wherein the module to graphically display the simulated scan flops versus time also displays the pseudo-signal.

14. (original) The article of manufacture of claim 11, the test program further including a module to form a pseudo-signal including data identifying miscompares between the simulated displayed scan flops and expected signal values derived from an automatic pattern generator, wherein the module to graphically display the simulated scan flops versus time is also configured to display the pseudo-signal.

15. (original) The article of manufacture of claim 11, wherein the module to extract the simulated scan flops of one or more scan chains from the output data includes a module to reduce the scope of the simulated output data to one scan chain to be analyzed.

16. (original) The article of manufacture of claim 11, wherein the module to extract the simulated scan flops of one or more scan chains from the simulated output data includes a module to reduce the scope of the simulated output data to one scan chain to be analyzed and wherein the module to sort the simulated extracted scan flops into a logical order is configured to sort the scan flops into a logical order extending from scan input to scan output.

17. (original) A computer implemented circuit simulation and fault detection system comprising:

memory configured to provide a database and operative to store a netlist including nets of an integrated circuit under design;

an automatic test pattern generation algorithm operative to generate test patterns to test an integrated circuit design; and

processing circuitry configured to simulate operation of the integrated circuit design to provide simulated circuit operation data and to identify types of defects occurring during simulation of the integrated circuit design and operative to: extract simulated scan flops from the simulated circuit operation data; sort the simulated scan flops into a logical order; identify labels for the simulated scan flops; and graphically display the simulated scan flops versus time together with the labels.

18. (original) The circuit simulation system of claim 17, wherein the processing circuitry comprises a processor configured to implement the automatic test pattern generation program.

19. (original) The circuit simulation system of claim 17, wherein the processing circuitry is further operative to graphically display the simulated scan enable signal.

20. (original) The circuit simulation system of claim 17, wherein the processing circuitry is further operative to form expected scan output data from the netlist using an automatic test pattern generator and form a pseudo-signal graphically displaying miscompares between the displayed simulated scan flops and the expected scan output data.

21. (original) The circuit simulation system of claim 17, wherein the processing circuitry is further operative to reduce the scope of the simulated output data to one scan chain to be analyzed.

22. (original) The circuit simulation system of claim 17, wherein the processing circuitry is further operative to reduce the scope of the output data to one scan chain to be analyzed and sort the simulated scan flops into a logical order extending from scan input to scan output.